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QUESTION WORKBOOK

Digital signal processing

Electronics · Year 13

AQA 3.13.5.1, 3.13.5.2, 3.13.5.3

17 questions · 50 marks

NAVY SCREEN EDITION

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SECTION A · Warm-up

A1 Explain why a digital signal is far less affected by noise on a long cable than an analogue signal carrying the same information. [2]

A2 State the difference between regenerating a digital signal and amplifying an analogue one. [2]

A3 Write out the truth table of an EOR gate, and state in one sentence what it does. [2]

A4 Write out the truth table of a NAND gate, and state its relationship to the AND gate. [2]

A5 Describe the behaviour of a D-type flip-flop. [2]

A6 State the relationship between the input and output frequencies of a chain of n toggling flip-flop stages. [1]

SECTION B · Standard

B1 A logic circuit has output Q = (A OR B) AND NOT C. Construct its full truth table, with the inputs in binary counting order, and state how many input combinations give Q = 1. [3]

B2 A chain of 10 toggling flip-flop stages is clocked at 1.024 MHz. Calculate the frequency at the output of the final stage. [3]

B3 A timing circuit is clocked at 2.048 MHz and must produce an output at 250 Hz. Calculate the number of toggling flip-flop stages required. [3]

B4 A binary counter is built from 6 toggling flip-flop stages and clocked at 4096 Hz. State the number of distinct states it passes through, the range of counts it displays, and the frequency at its final output. [3]

B5 A half-adder adds two single binary digits A and B. Name the gate that produces each of its two outputs, and give the sum and carry for every combination of the inputs. [3]

B6 An alarm sounds (Q = 1) when a door is open (D = 1) and the system is armed (R = 1) and the override key is not inserted (K = 0). Write the Boolean expression, name the gates required, and give Q for the three cases D = 1, R = 1, K = 0; D = 1, R = 1, K = 1; and D = 0, R = 1, K = 0. [3]

B7 A logic system uses 0 V for logic 0 and 5.0 V for logic 1, with a decision threshold at 2.5 V. A pulse sent at 4.6 V arrives with 0.9 V of noise subtracted from it. State the voltage at the receiver, and state whether the pulse is read correctly. [2]

SECTION C · Stretch

C1 A pump must run (P = 1) when the tank level is low (L = 1), unless the manual stop is pressed (S = 1). It must also run whenever the test button is pressed (T = 1), whatever the other two inputs are doing. Construct the full truth table, write the Boolean expression, name the gates needed, and state how many of the eight input combinations run the pump. [7]

C2 A quartz watch runs from a crystal at 4 194 304 Hz. Calculate the number of toggling stages needed to produce a once-per-second tick, and calculate the frequency available at the output of the twelfth stage. [4]

C3 A full adder adds two bits A and B together with a carry brought in from the column to its right. It is built from two half-adders and an OR gate. Explain how the two half-adders are connected, and give the sum and carry outputs when A = 1, B = 1 and the incoming carry is 1. [4]

C4 A digital link uses 0 V and 5.0 V logic levels with the threshold midway. Noise accumulates at 0.35 V per kilometre of cable, and the receiver is reliable while the accumulated noise stays below 1.2 V. Calculate the greatest whole number of kilometres between regenerators, and the number of regenerators needed on a 30 km route. Explain why an analogue link over the same route cannot be rescued the same way. [4]